

REMARKS

Independent claims 1, 22, and 30 are amended to include limitations that further specify characteristics of the low-level design representation and the high-level design representation. Specifically, the low-level design representation includes Boolean equations and no IF statement, and the high-level design representation is an HDL that has an IF statement. Support for the amendments may be found in paragraphs [0004], [0032], [0034], and FIGs. 5A, 6A-C, 8A-C. Claims 7, 9, 19, 21, and 27 are cancelled, and dependent claims 28 and 29 are amended for consistency with the base claim 22.

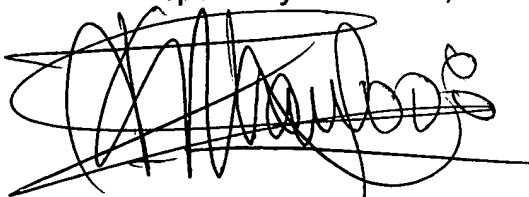
Claims 1-6, 8, 10-18, 20, 22-26, and 28-30 remain, and reconsideration and allowance of the application are respectfully requested.

The rejection of claims 1-30 under 35 USC §102(e) as being anticipated by "Bennett" (US patent number 5,659,484 to Bennett et al.) is respectfully traversed because all the limitations are not shown to be taught by Bennett. Furthermore, the rejection is moot in view of the amendments to the claims. It will be recognized that Bennett's system is not shown to teach transforming of a low-level Boolean equation representation that has no IF statement to a high-level representation in an HDL that has an IF statement. For example, Bennett's Boolean equations in FIG. 7, #306 neither appear to be low-level, nor do they appear to be translated into an HDL having an IF statement such the VHDL which is also in FIG. 7, #306. Therefore, the limitations of the claims are not shown to be taught by Bennett, and withdrawal of the rejection is respectfully requested.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Keith A. Chanroo', written over a horizontal line.

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 27, 2006.

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